CLAIM OR CLAIMS

WHAT IS CLAIMED IS:

1. An instrument receiver architecture comprising:

a low-band IF channel having as an input an RF signal and providing as an output a low-band IF signal;

a bank of preselection filters having as an input the RF signal and providing as an output a selected frequency band of the RF signal;

a high-band IF channel having as an input the selected frequency band and providing as an output a high-band IF signal; and

means for selecting one of the low-band and high-band IF signals for further processing.

2. The architecture as recited in claim 1 wherein the low-band IF channel comprises:

an up-converting stage having the RF signal as an input and providing as an output a first IF signal; and

a down-converting stage having the first IF signal as an input and providing as an output a second IF signal, the second IF signal being the low-band IF signal for input to the selecting means.

3. The architecture as recited in claim 2 wherein the high-band IF channel comprises a hi-band down-converting stage having as an input the selected frequency band and providing as an output the high-band IF signal for input to

the selecting means, the high-band IF signal having the same intermediate frequency as the low-band IF signal.

4. The architecture as recited in claim 1 wherein the low-band IF channel comprises an up-converting stage having as an input the RF signal and providing as an output the low-band IF signal for input to the selecting means.

5. The architecture as recited in claim 4 wherein the high-band IF channel comprises a down-converting stage having as an input the selected frequency band and providing as an output the high-band IF signal for input to the selecting means, the low-band and high-ban IF signals having different intermediate frequencies.

6. The architecture as recited in claim 5 further comprising an output down-converting stage coupled to the selecting means, the output down-converting stage being configurable to convert both the low-band and high-band IF signals to a common IF signal for further processing.

7. The architecture as recited in claim 6 wherein the output down-converting stage comprises:

a mixer having an input coupled to the selecting means and providing as an output the common IF signal;

a local oscillator providing a first local oscillator signal for mixing with the low-band IF signal when selected by the selecting means and a second

local oscillator signal for mixing with the high-band IF signal when selected by the selecting means, the first local oscillator signal having a frequency higher than the frequency of the second local oscillator signal and the low-band IF signal having a higher intermediate frequency than the high-band IF signal.

8. The architecture as recited in claim 7 wherein the local oscillator comprises:

an oscillator having as an output the first local oscillator signal; and

means for deriving the second local oscillator signal from the first local oscillator signal.

9. The architecture as recited in claim 8 wherein the deriving means comprises a divider having as an input the first local oscillator signal and having as an output the second local oscillator signal.

10. The architecture as recited in claim 1 wherein the low-band IF channel comprises:

a low-band bank of preselection filters having as an input the RF signal and providing as an output a selected frequency band of the RF signal; and

a low-band converter stage having as an input a selected one of the RF signal and the selected frequency band and having as an output the low-band IF signal for input to the selecting means, the low-band converter stage operating as an up-converting stage when the input is the RF signal to produce an up-converted low-band IF signal as the low-band IF signal and

operating as a low-band down-converting stage when the input is the selected frequency band to produce a down-converted low-band IF signal as the low-band IF signal.

11. The architecture as recited in claim 10 wherein the high-band IF channel comprises a down-converting stage having as an input the selected frequency band and providing as an output the high-band IF signal for input to the selecting means.

12. The architecture as recited in claim 11 wherein the selecting means comprises:

a first means for selecting as an output one of the high-band IF signal and the down-converted low-band IF signal; and

a second means for selecting as an output one of the high-band IF signal and the up-converted low-band IF signal.

13. The architecture as recited in claim 12 further comprising an output down-converting stage for converting the output from the first and second selecting means to a common IF signal for further processing.

14. The architecture as recited in claim 13 wherein the output down-converting stage comprises:

a mixer having as an input the output from the first and second selecting means and providing as an output the common IF signal;

a local oscillator providing as outputs a first local oscillator signal for mixing with the up-converted low-band IF signal when selected by the first and second selecting means to produce the common IF signal and a second local oscillator signal for mixing with the selected one of the high-band IF signal and the down-converted low-band IF signal when selected by the first and second selecting means to produce the common IF signal, the first local oscillator signal having a frequency higher than the frequency of the second local oscillator signal and the up-converted low-band IF signal having a higher intermediate frequency than the down-converted low-band and high-band IF signals.

15. The architecture as recited in claim 14 wherein the local oscillator comprises:

an oscillator having as an output the first local oscillator signal; and

means for deriving the second local oscillator signal from the first local oscillator signal.

16. The architecture as recited in claim 15 wherein the deriving means comprises a divider as an input having the first local oscillator signal and having as an output the second local oscillator signal.

17. The architecture as recited in any of claims 1-16 further comprising a tunable local oscillator having as outputs a first oscillator frequency signal for input to the low-band IF channel to produce the low-band IF signal and a

second oscillator frequency signal for input to the high-band IF channel to produce the high-band IF signal, the second local oscillator frequency signal having a frequency that is higher than the frequency of the first local oscillator frequency signal.

18. The architecture as recited in claim 17 wherein the tunable local oscillator comprises:

a YIG tunable oscillator having as an output the second oscillator frequency signal; and

means for deriving the first oscillator frequency signal from the second oscillator frequency signal.

19. The architecture as recited in claim 18 wherein the deriving means comprises a divider having as an input the second oscillator frequency signal and having as an output the first oscillator frequency signal.